ABSTRACT

A packaged chip-scale semiconductor device (400) has a substrate with a patterned metal layer (202) and first and second surfaces (202a and 202b, respectively). The first portion of an insulating material (305a) fills the spaces of the patterned metal layer. The second portion (401) of the insulating material is attached to the first surface (202a) of the patterned metal layer, forming a plurality of windows (402) to expose the metal for connection to external parts; around the periphery of these windows, the insulating material (401) preferably has a thickness of less than 30 μm. The third portion (205) of the insulating material forms, on the second surface (202b) of the patterned metal layer, a layer with an area suitable for attaching an integrated circuit chip (206). Solder balls attached to the metal surfaces exposed in the windows (402) have solder necks after reflow preferably less than 30 μm long, which helps avoid a solder separation problem induced by surface tension.